Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Please amend claims 1-10, as follows:

1. (Currently Amended) A controller for controlling interruption and restarting of data writing to a recording medium, wherein the data written to the recording medium is read from a buffer memory, the controller comprising:

an encoder connected to the buffer memory, wherein the encoder receives the data read from the buffer memory and encodes the read data to generate encoded data;

a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data when the writing of data to the recording medium is interrupted;

a first retry determination circuit for determining whether an address of the ~~write~~ written data, which is read from the recording medium, and an address of the read data, which is provided to the encoder from the buffer memory, ~~match~~ are the same;

a second retry determination circuit for determining whether a timing for reading the ~~write~~ written data from the recording medium and a timing for encoding the read data ~~match~~ are the same; and

a restart circuit for restarting the writing of data to the recording medium based on the determinations of the first and second retry determination circuits.

2. (Currently Amended) The controller according to claim 1, wherein the second retry determination circuit determines whether the timings ~~match~~ are the same when the first retry determination circuit determines that the addresses ~~match~~ are the same.

3. (Currently Amended) A controller for controlling interruption and restarting of data writing to a recording medium, wherein the data written to the recording medium is read from a buffer memory, the controller comprising:

an encoder connected to the buffer memory, wherein the encoder receives the data read from the buffer memory and encodes the read data to generate encoded data;

one or more address memories connected to the buffer memory, wherein the one or more address memories store a write data address of the data written to the recording medium and a read data address of the data read from the buffer memory when the writing of data to the recording medium is interrupted, wherein the write data address and the read data address each indicate a location of the data when the interruption occurs;

a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data;

a first retry determination circuit for determining whether an address of the written data, which is read from the recording medium, and the write data address, which is stored in the one or more address memories, ~~match~~ are the same, and for determining whether an address of the read data, which is provided to the encoder from the buffer memory, and the read data address, which is stored in the one or more address memories, ~~match~~ are the same;

a second retry determination circuit for determining whether a timing for reading the written data from the recording medium and a timing for encoding the read data ~~match~~ are the same; and

a restart circuit for restarting the writing of data to the recording medium based on the determinations of the first and second retry determination circuits.

4. (Currently Amended) The controller according to claim 3, wherein the written data read from the recording medium includes a first subcode synchronizing signal and the encoded data includes a second subcode synchronizing signal, and wherein the second retry determination circuit determines whether the timing for reading the written data from the recording medium and the timing for encoding the read data ~~match~~ are the same based on the

first and second subcode synchronizing signals.

5. (Currently Amended) The controller according to claim 3, wherein the second retry determination circuit determines whether the timings ~~match~~ are the same when the first retry determination circuit determines that the addresses ~~match~~ are the same.

6. (Currently Amended) The controller according to claim 3, further comprising:

a first location detection circuit connected to the one or more address memories, wherein the first location detection circuit detects whether the address of the written data read from the recording medium ~~matches~~ and the write data address stored in the one of more address memories are the same; and

a second location detection circuit connected to the one or more address memories, wherein the second location detection circuit detects whether the address of the data read from the buffer memory ~~matches~~ and the read data address stored in the one or more address memories are the same.

7. (Currently Amended) A controller for controlling interruption and restarting of data writing to a recording medium, wherein the data written to the recording medium is read from a buffer memory, the controller comprising:

an encoder connected to the buffer memory, wherein the encoder receives data read from the buffer memory and encodes the read data to generate encoded data;

one or more address memories connected to the buffer memory, wherein the one or more address memories store a write data address of the data written to the recording medium and a read data address of the data read from the buffer memory when the writing of data to the recording medium is interrupted, wherein the write data address and the read data address each indicate a location of the data when the interruption occurs;

a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data;

a retry determination circuit for determining whether an address of the written data, which is read from the recording medium, and the write data address, which is stored in the one or more address memories, ~~match~~ are the same, and for determining whether an address of the read data, which is provided to the encoder from the buffer memory, and the read data address, which is stored in the one or more address memories, ~~match~~ are the same, wherein the synchronizing circuit determines whether a timing for reading the written data from the recording medium and a timing for encoding the read data ~~match~~ are the same; and

a restart circuit for restarting the writing of data to the recording medium based on the determinations of the retry determination circuit and the synchronizing circuit.

8. (Currently Amended) The controller according to claim 7, wherein the written data read from the recording medium includes a first subcode synchronizing signal and the encoded data includes a second subcode synchronizing signal, and wherein the synchronizing circuit determines whether the timing for reading the written data from the recording medium and the timing for encoding the read data ~~match~~ are the same based on the first and second subcode synchronizing signals.

9. (Currently Amended) The controller according to claim 7, wherein the synchronizing circuit determines whether the timings ~~match~~ are the same when the first retry determination circuit determines that the addresses ~~match~~ are the same.

10. (Currently Amended) The controller according to claim 7, further comprising:

a first location detection circuit connected to the one or more address memories, wherein the first location detection circuit detects whether the address of the written data read from the recording medium ~~matches~~ and the write data address stored in the one of more address memories are the same; and

a second location detection circuit connected to the one or more address memories, wherein the second location detection circuit detects whether the address of the data read from

the buffer memory ~~matches~~ and the read data address stored in the one or more address memories are the same.